[resistance] resistivity [, positioned] arranged close to said [insulation] insulating layer [and having a second conductive type opposite to said first conductive type], [and] a second channel area of the first conductivity type and of a high [resistance] resistivity[, having said first conductive type and positioned adjacent] arranged close to said first channel area, and a third channel area of the second conductivity type arranged close to said second channel area, said third channel area is arranged close to an additional insulating layer, and an electrically neutral area is formed in said third channel area at a side adjacent to said additional insulating area.

Please cancel Claim 2 without prejudice or disclaimer of subject matter.

Please amend Claim 5 as follows:

5. (Amended) A semiconductor device according to Claim 1, wherein said [semiconductor layer is formed on an] additional insulating [member] layer is an insulative substrate.

Please cancel Claims 6, 9 and 10 without prejudice or disclaimer of subject matter.

Please amend Claim 11 as follows:

11. (Amended) A semiconductor device [according to Claim 9,] provided at least with a semiconductor layer including source and drain areas of a first conductive type and of a high impurity concentration and a channel area

positioned between said source and drain areas, an insulation layer covering at least said channel area, and a gate electrode positioned close to said insulation layer, wherein said channel area at least comprises a first channel area of a low resistance, positioned close to said insulation layer and having a second conductive type opposite to said first conductive type, and a second channel area of a high resistance, having said first conductive type and positioned adjacent to said first channel area, and [wherein said channel area] further comprises a [third channel] area of the second conductive type, positioned adjacent to said second channel area, said semiconductor device constituting an integrated circuit including an MIS transistor comprising a [fourth] channel area of the first conductive type, positioned between the first and second channel areas.

Please cancel Claims 12 and 13 without prejudice or disclaimer of subject matter.

Please amend Claim 19 as follows:

19. (Amended) A semiconductor device according to Claim [9] 1, wherein the impurity concentration of said third channel area is within a range of $10^{14}$ to $10^{18}$ $cm^{-3}$.

Please add Claims 20-42 as follows:

--20. A semiconductor device according to Claim 1, further comprising an additional gate electrode on said third channel across said additional insulating layer.

21. A semiconductor device according to claim 11, wherein the impurity concentration of said fourth channel area is higher than that of said second area.

22. A semiconductor device according to Claim 11, wherein the impurity concentration of said fourth channel area is lower than that of said second area.

23. A semiconductor device according to Claim 11, wherein the MIS transistor is formed so that, when a voltage is applied to the gate, a potential distributed in the channel region is higher, and a carrier flows at a position distant from an interface between the insulating layer and the first channel area by a distance longer than a mean free path of the carrier.

24. A semiconductor device according to Claim 23, wherein said MIS transistor is of an enhancement type.

25. A semiconductor device according to Claim 11, wherein an impurity concentration in said source and drain regions is $10^{18}$-$10^{21}$ $cm^{-3}$.

26. A semiconductor device according to Claim 11, wherein the impurity concentration in said first channel area is $10^{15}$-$10^{19}$ $cm^{-3}$.

27. A semiconductor device according to Claim 11, wherein the impurity concentration in said second or fourth channel area is not greater than $10^{17}$ $cm^{-3}$.

28. A semiconductor device according to Claim 11, wherein the first conductivity type is n.

29. A semiconductor device according to Claim 11, wherein the second conductivity type is p.

30. A semiconductor device according to Claim 11, wherein the impurity concentration in said [third channel area] is $10^{14}$-$10^{18}$ $cm^{-3}$.

31. A semiconductor device provided at least with source and drain regions of a first conductivity type and of a high impurity concentration, a semiconductor layer including a channel region between said source and drain regions, an insulating layer at least on said semiconductor layer, and a gate electrode on said insulating layer, wherein at least said semiconductor layer comprises a first area of low resistivity and of a second conductivity type opposite to the first conductivity type adjacent to said insulating layer, a [fourth] area of the first conductivity type adjacent to the first area, a second area of the first conductivity type adjacent to said [fourth] area, and a [third channel area] of the second conductivity type adjacent to said second area.

32. A semiconductor device according to claim 31, wherein the impurity concentration of said [fourth] area is higher than that of said second area.

33. A semiconductor device according to Claim 31, wherein the impurity concentration of said [fourth] area is lower than that of said second area.

34. A semiconductor device according to Claim 31, further comprising

an MIS transistor formed so that, when a voltage is applied to the gate, a potential distributed in the channel region is higher, and a carrier flows at a position distant from an interface between the insulating layer and the first area by a distance longer than a mean free path of the carrier.

35. A semiconductor device according to Claim 34, wherein said MIS transistor is of an enhancement type.

36. A semiconductor device according to Claim 31, wherein an impurity concentration in said source and drain regions is $10^{18}$-$10^{21}$ $cm^{-3}$.

37. A semiconductor device according to Claim 31, wherein the impurity concentration in said first area is $10^{15}$-$10^{19}$ $cm^{-3}$.

38. A semiconductor device according to Claim 31, wherein the impurity concentration in said second or [fourth] third area is not greater than $10^{17}$ $cm^{-3}$.

39. A semiconductor device according to Claim 31, wherein the first conductivity type is n.

40. A semiconductor device according to Claim 31, wherein the second conductivity type is p.

41. A semiconductor device according to Claim 31, wherein the impurity concentration in said [third] substrate area is $10^{14}$-$10^{18}$ $cm^{-3}$.--